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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Kurt A. Summe
Wood, Herron & Evans, L.L.P.
2700 Carew Tower
441 Vine Street
Cincinnati, OH 45202-2917

EXAMINER	
VU, PHUONG T	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 01/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/085,170	BAKER, PETER T.
	Examiner	Art Unit
	Phuong T. Vu	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 24-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 24-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8, 10-12, 16, 24-25, 27, 35-37, 40-43, 45-46 are rejected under 35 U.S.C. 102(b), or in the alternative, under 35 U.S.C. 103(a) as being unpatentable over McSparran et al. (US 4,658,334). Regarding claim 1, the reference notes that it pertains to electronic systems which provide RF isolation and shielding (column 1, lines 2-27). It further states that such systems include high gain amplifiers and high gain preamplifiers.

The reference discloses a power amplifier system comprising a single circuit board 100 having a plurality of subcircuits thereon which includes a gain subcircuit thereon, the circuit board comprising multiple conductive layers 110-114 including a first signal distribution layer 111, a second ground layer 110 and a third signal layer distribution layer 112 embedded in the circuit board, the second ground plane layer

disposed between the first and third signal distribution layers, a chassis body (bottom component 30) and a lid structure (top component 30) for coupling with the chassis body to contain the circuit board, and a wall 37, 33 extending from the lid structure and surrounding a subcircuit to electrically isolate the subcircuit from other subcircuits on the circuit board.

Regarding claim 2, the gain subcircuit is a high power gain subcircuit and the wall surrounds the high power gain subcircuit.

Regarding claim 3, the wall forms a cavity 31 or 32 for containing the subcircuit.

Regarding claim 4, the circuit board includes a ground path 132-13 formed along a surface of the board, the wall coupling with a portion of the ground path for grounding the wall and the lid structure.

Regarding claim 5, the ground path is shaped to surround a portion of the subcircuit, the wall having a shape generally corresponding to the shape of the ground path.

Regarding claim 6, the multiple conductive layers are separated by a dielectric layer 121, the first conductive layer being coupled to components of the subcircuits and the second conductive layer defining a ground plane.

Regarding claim 7, the reference teaches that the third signal layer is separated from the second ground plane layer by a dielectric layer 122 and is configured for distributing signals across the circuit board and between subcircuit components.

Regarding claim 8, a fourth conductive layer 114 is separated from the third signal distribution layer by a dielectric layer 124 and defining a ground plane 132-14.

Regarding claim 10, the fourth conductive layer is electrically coupled to the chassis body.

Regarding claim 11, the fourth conductive layer is substantially metallized.

Regarding claim 12, the lid structure includes component clearance areas 31, 32 adapted to provide clearance for components of the subcircuits.

Regarding claim 16, the chassis body includes at a least one channel 31 or 32 adapted to contain at least one subcircuit extending downwardly from the circuit board.

Regarding claim 24, the reference discloses a power amplifier comprising a multiple-layer circuit board having a plurality of subcircuits, including a gain subcircuit, thereon; the circuit board comprising multiple conductive layers 110-114 including a first signal distribution layer 111, a second ground layer 110 and a third signal layer distribution layer 112 embedded in the circuit board, the second ground plane layer disposed between the first and third signal distribution layers, a chassis body (bottom component 30) and a lid structure (top component 30) for coupling with the chassis body to contain the circuit board, the circuit board ground plane layer being electrically coupled to the chassis body, a plurality of plated vias (134, 164, also refer to col 5, lines 1-8) extending through the circuit board to electrically carry signals and ground between the layers, some of the plurality of vias forming a ground isolation path positioned between the at least two subcircuits on the circuit board, at least one wall 37, 33 extending from the lid structure and coupled to the ground isolation path to electrically isolate the subcircuit from the other subcircuits on the circuit board. Since the subcircuit

contains the gain subcircuit, it would necessarily be isolated from the other subcircuits for EMI suppression.

Regarding claim 25, the multiple conductive layers are separated by dielectric layers, a first conductive layer being coupled to components of the subcircuits and the second conductive layer defining the ground plane.

Regarding claim 27, the lid structure wall coupled to the ground isolation path and has a shape generally corresponding to the ground isolation path.

Regarding method claims 35-37, 40-43, 45-46, one would necessarily perform the recited steps in the manufacture of the apparatus rejected above.

4. Claims 9, 15, 26, 28, 34, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over McSparran et al. (US 4,658,334). Regarding claim 9, the reference speaks only generally of gain amplifier circuitry but does not provide detail about specific circuitry. It would have been obvious to those skilled in the art at the time the invention was made that one of the signal distribution layers, including the first signal distribution layer would include at least some circuitry which may be considered a controlled impedance circuit as gain amplifiers typically include controlled impedance circuits coupled to the output of the amplifiers to function as feedback networks. Utilizing the ground plane of the second layer to complete circuits is expedient in the art. The examiner takes Official Notice.

Regarding claims 15, 26, the reference does not teach providing a gasket coupled to the wall and positioned between the wall and the ground isolation path for

further providing isolation. Use of gaskets in such a configuration for providing radio frequency shielding is expedient in the art.

Regarding claim 28, the reference discloses a power amplifier comprising a single circuit board 100 having a plurality of subcircuits thereon which includes a high power gain subcircuit thereon, the circuit board comprising multiple signal distribution layers 111-114 with at least one signal distribution layer 112 embedded in the circuit board and a ground plane layer 110 disposed between the signal layer distribution layers, a chassis body (bottom component 30) and a lid structure (top component 30) for coupling with the chassis body to contain the circuit board, and a wall 37, 33 extending from the lid structure and surrounding a subcircuit to electrically isolate the subcircuit from other subcircuits on the circuit board. The reference speaks only generally of gain amplifier circuitry but does not provide detail about specific circuitry. It would have been obvious to those skilled in the art at the time the invention was made to provide a power supply subcircuit to provide power to the amplifier and to position this power supply subcircuit along with the other subcircuits so they would necessarily be isolated from the high power gain subcircuit.

Regarding claim 29, the circuit board includes an isolation ground path 132-14 formed along a surface of the board, the wall coupling with a portion of the isolation ground path.

Regarding claim 30, the isolation ground path is shaped to surround a portion of the subcircuits and the wall has a shape generally corresponding to the shape of the isolation ground path.

Regarding claim 31, the ground isolation path is electrically coupled with the chassis body.

Regarding claim 32, the ground isolation path includes a plurality of plated vias extending into the circuit board.

Regarding claim 33, the multiple conductive layers are separated by dielectric layers, the signal distribution layers being coupled to components of the subcircuits and the ground plane layer defining a ground plane

Regarding claim 34, those skilled in the art would recognize that the power supply subcircuit and the high power gain subcircuit should be positioned as far away from each other on the circuit board to minimize electromagnetic interference.

Regarding method claim 39, one would necessarily perform the recited steps in the manufacture of the apparatus rejected above.

5. Claims 13-15, 26, 38, 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over McSparran et al. (US 4,658,334) in view of Pressler et al. (US 5,550,713).

Regarding claims 13-14, McSparran does not show that the chassis body includes at one coupling channel/pathway formed therein to allow coupling connections between subcircuits. However, Pressler teaches that it is known to provide coupling channels 101 for coupling connections between subcircuits in an assembly comprising a circuit board 50 with a plurality of subcircuits, a chassis body 84 and a lid structure 82 for coupling with the chassis body, and at least one wall 88 extending from the lid structure and surrounding the subcircuit to electrically isolate the subcircuit from other

subcircuits on the circuit board. It would been obvious to those skilled in the art at the time the invention was made to provide at least one coupling channel/pathway formed in the wall of the chassis body for allowing convenient coupling connections between the subcircuits on the outer surface board as taught by Pressler.

Regarding claims 15, 26, McSparran does not show providing a gasket is coupled to the wall for further isolating the subcircuit. However, Pressler teaches providing gasket 105 coupled to a wall of a cover and positioned between the wall and the ground isolation path for further isolating a subcircuit of circuit board. It would have been obvious to those skilled in the art at the time the invention was made to provide a gasket as shown by Pressler to provide a more effective seal between the wall and the circuit board for better EMI shielding protection.

Regarding method claims 38, 44, one would necessarily perform the recited steps in the manufacture of the apparatus rejected above.

Conclusion

6. Applicant's arguments with respect to the have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong T. Vu whose telephone number is (703) 308-0303. The examiner can normally be reached on Mon. & Tues., 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Martin be reached on (703) 308-3121. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PTVu
January 22, 2003

Jayprakash N. Gandhi
Primary Examiner
Technology Center 2800